Remarks

I. Status of Claims

Claims 14-21 were pending.

Claims 22-36 have been added.

II. Claim Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 14-18, 20, and 21 under 35 U.S.C. § 102(b) over Wilson (U.S. 4,980,157). In particular, the Examiner has asserted that:

> Wilson teaches adhering an unprocessed, integratable form of a plurality of chips on the upper surface of a carrier substrate according to a first placement alignment precision (col . 7, lines 34-54). Wilson discloses lithographically processing the unprocessed, integrateable form of a plurality of chips on the upper surface (Abstract, col. 2, lines 35-68, col. 7, lines 34-54). Wilson shows the integrated chips being aligned with each other and the substrate with a second alignment precision having lithographic processing tolerances (col. 7, lines 34-54). Wilson describes the lithographic processing tolerance being ±1 micron and the overlay tolerance of ±1 mil. (col. 7, lines 34-54). Wilson teaches forming a plurality of alignment holes (slots) and adhering by using alignment pins to mate with corresponding the alignment holes (col. 2, lines 65-68, col. 3, lines 1-10, col. 6, lines 38-68, col. 7, lines 1-12). Wilson discloses using the casting method (curtain coating deposition) as part of the lithographically processing (col. 2, lines 45-47, col. 3, lines 65-68, col. 4, line 1). Wilson teaches the upper surface of the integrated chips being directly formed in parallel, but different plane than the substrate carrier (col. 2, lines 35-4, col. 7, lines 15-50).

As explained in detail below, the Examiner's rejection of claims 14-18, 20, and 21 is based on a misreading of Wilson's disclosure.

A. Independent Claim 14

Independent claim 14 recites:

> 14. A method of forming a common carrier comprising the steps of:
>
> adhering an unprocessed, integrateable form of a plurality of chips on the upper surface of a carrier substrate according to a first placement alignment precision;
>
> lithographically processing the unprocessed, integrateable form of the plurality of chips to form a plurality of integrated chips on the upper surface, wherein the integrated chips are aligned with each other and the substrate with a second alignment precision having lithographic processing tolerances.

Contrary to the Examiner's assertion, Wilson does not adhere unprocessed integrateable forms of a plurality of chips on the upper surface of a carrier substrate. Instead, the integrated circuit chips 30 that are affixed to the upper surface of a multilayer film 17 in accordance with Wilson's teachings are completely processed into integrated circuit chips before they are affixed to the multilayer film 17. In particular, Wilson teaches that (col. 2, lines 57-65):

> After formation of the film has been completed, it is cured in a final cure process at 450° C, in an inert atmosphere to completely convert the polyamic acid resin to a polyimide film and to anneal the micropolymer structure. Integrated circuit chips are then soldered to the conductors of the film, and the entire assembly is then removed from the substrate by subjecting the film assembly and substrate to an appropriate chemical swelling agent.

Wilson does not teach or suggest anything that would have led one of ordinary skill in the art at the time the invention was made to believe that the integrated circuit chips 30 are "an unprocessed, integrateable form of a plurality of chips," are recited in claim 14.

In addition, Wilson does not teach or suggest "lithographically processing the unprocessed, integrateable form of the plurality of chips to form a plurality of integrated chips on the upper surface," as recited in claim 14. Indeed, the integrated circuit chips 30 have been completely processed into integrated circuit chips before they are affixed to the multilayer film 17. Therefore, in accordance with Wilson's teachings, the integrated circuit chips 30 are not processed after they have been affixed to the multilayer film 17.

For at least these reasons, the Examiner's rejection of independent claim 14 under 35 U.S.C. § 102(b) over Wilson should be withdrawn.

B. Claims 15-18, 20, and 21

Each of claims 15-18, 20, and 21 incorporates the features of independent claim 14 and therefore is patentable over Wilson for at least the same reasons explained above. Claims 15-18 also are patentable over Wilson for the following additional reasons.

1. Claim 15

Claim 15 recites that "the first alignment precision has a greater tolerance range than the lithographic processing tolerances."

The Examiner states that "Wilson describes the lithographic processing tolerance being ±1 micron and the overlay tolerance of ±1 mil (col. 7, lines 34-54)." Contrary to the Examiner's implication, however, these tolerance ranges do not respectively correspond to the tolerance range with which the integrated circuit chips 30 are processed on the multilayer film 17 and the tolerance range with which the integrated circuit chips 30 are adhered to the multilayer film 17. Instead, the tolerance range of ±1 μm corresponds to the alignment tolerance that is theoretically achievable between the alignment holes that are formed in the multilayer film 17 and the alignment holes for the alignment pins 43, 45 and the integrated circuit chips 30 that are formed in the template 40, assuming that there were no compensation requirements. The tolerance range of ±1 mil (which is equal to one thousandth of an inch, or 25.4 μm) corresponds to the actual alignment tolerance range between the 20 mil alignment circles in the template 40 and the 30 mil alignment squares in the multilevel film substrate 10 that is achievable for an implementation of Wilson's circuit product given the compensation requirements.

As explained above, Wilson does not process the integrated circuit chips 30 after they are affixed to the multilayer film 17. For this reason, Wilson does not teach or suggest anything about the tolerance range of such processing. In addition, Wilson does not specify a tolerance range for the alignment precision with which the integrated circuit chips 30 are adhered to the multilayer film 17.

2. Claim 16

Claim 16 recites that "the first alignment precision has a tolerance in the range of +/-1 milimeter and the second alignment precision has a tolerance in the range of less than 1 micron."

Wilson does not teach or suggest the features recited in claim 16 for the same reasons explained above in connection with claim 15.

3. Claim 17

Claim 17 recites: "forming a plurality of slots within the upper surface of the carrier substrate according to the first alignment precision; and adhering the unprocessed, integrateable form of the integrated chips within the plurality of slots."

With regard to claim 17, the Examiner has asserted that "Wilson teaches forming a plurality of alignment holes (slots) and adhering by using alignment pins to mate with corresponding the alignment holes (col. 2, lines 65-68, col. 3, lines 1-10, col. 6, lines 38-68, col. 7, lines 1-12).

The Examiner, however, has misread claim 17. Claim 17 does not recite "adhering by using alignment pins to mate with corresponding the alignment holes." Instead, claim 17 clearly recites "adhering the unprocessed, integrateable form of the integrated chips within the plurality of slots." As explained above, Wilson does not adhere unprocessed integrateable forms of a plurality of chips on the upper surface of a carrier substrate. Wilson most certainly does not adhere unprocessed integrateable forms of a plurality of chips within the alignment pin holes 54, 55 in the multilayer film 17 and the substrate 10.

4. Claim 18

Claim 18 incorporates the features of claim 17 and therefore is patentable over Wilson for at least the same reasons. Claim 18 also is patentable for the following additional reasons.

Claim 18 recites "depositing a filler so as to fill a peripheral gap between the interior edges of each of the slots and the peripheral edges of each of the unprocessed, integrateable form of the integrated chips when each unprocessed chip is adhered within each slot."

In her rejection, the Examiner has failed to address the features of claim 18 and therefore has failed to establish a proper *prima facie* case of obviousness with respect to this claim (see MPEP§ 706.02(j)).

In addition, Wilson does not teach or suggest "adhering the unprocessed, integrateable form of the integrated chips within the plurality of slots," as recited in claim 17. Consequently, there is no reason whatsoever for Wilson to teach "depositing a filler so as to fill a peripheral gap between the interior edges of each of the slots and the peripheral edges of each of the unprocessed, integrateable form of the integrated chips when each unprocessed chip is adhered within each slot," as recited in claim 18.

III. Claim Rejections under 35 U.S.C. § 102

The Examiner has rejected claim 19 under 35 U.S.C. § 103(a) over Wilson in view of Leibovitz (U.S. 5,055,425).

Claim 19 incorporates the features of independent claim 14. Leibovitz does not make-up for the failure of Wilson to teach or suggest the features recited in claim 14. Indeed, the Examiner has cited Leivovitz only for his disclosure of "using polishing to remove surface irregularities and prepare the surface of subsequent processing." Therefore, claim 19 is patentable over Wilson and Leibovitz for at least the same reasons explained above in connection with claim 14.

IV. New claims

New claim 22 is an independent claim. Each of new claims 23-36 depends from independent claim 22.

Independent claim 22 recites:

> 22. A method of forming a common carrier, comprising:
>
> providing a carrier substrate;
>
> adhering chip substrates to the carrier substrate at different respective locations across the carrier substrate, wherein alignment between the adhered chip substrates is within a first alignment tolerance range; and

lithographically processing the adhered chip substrates to form respective integrated structures on the adhered chip substrates, wherein alignment between the integrated structures respectively supported by different ones of the adhered chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range.

As explained above in connection with claim 14, in accordance with Wilson's teachings, the integrated circuit chips 30 have been completely processed into integrated circuit chips before they are affixed to the multilayer film 17. For this reason, the integrated circuit chips 30 are not processed after they have been affixed to the multilayer film 17.

Each of claims 23-36 incorporates the features of independent claim 22.

V. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 08-2025.

Respectfully submitted,

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